Nanotechnologies for computing and communications

A presentation to the

“Jornada de Seguimiento de Proyectos en Tecnologías y Diseño Electrónico”.

“Congreso en Diseño de Circuitos Electrónicos DCIS-2002.”

Jose A. Maiz

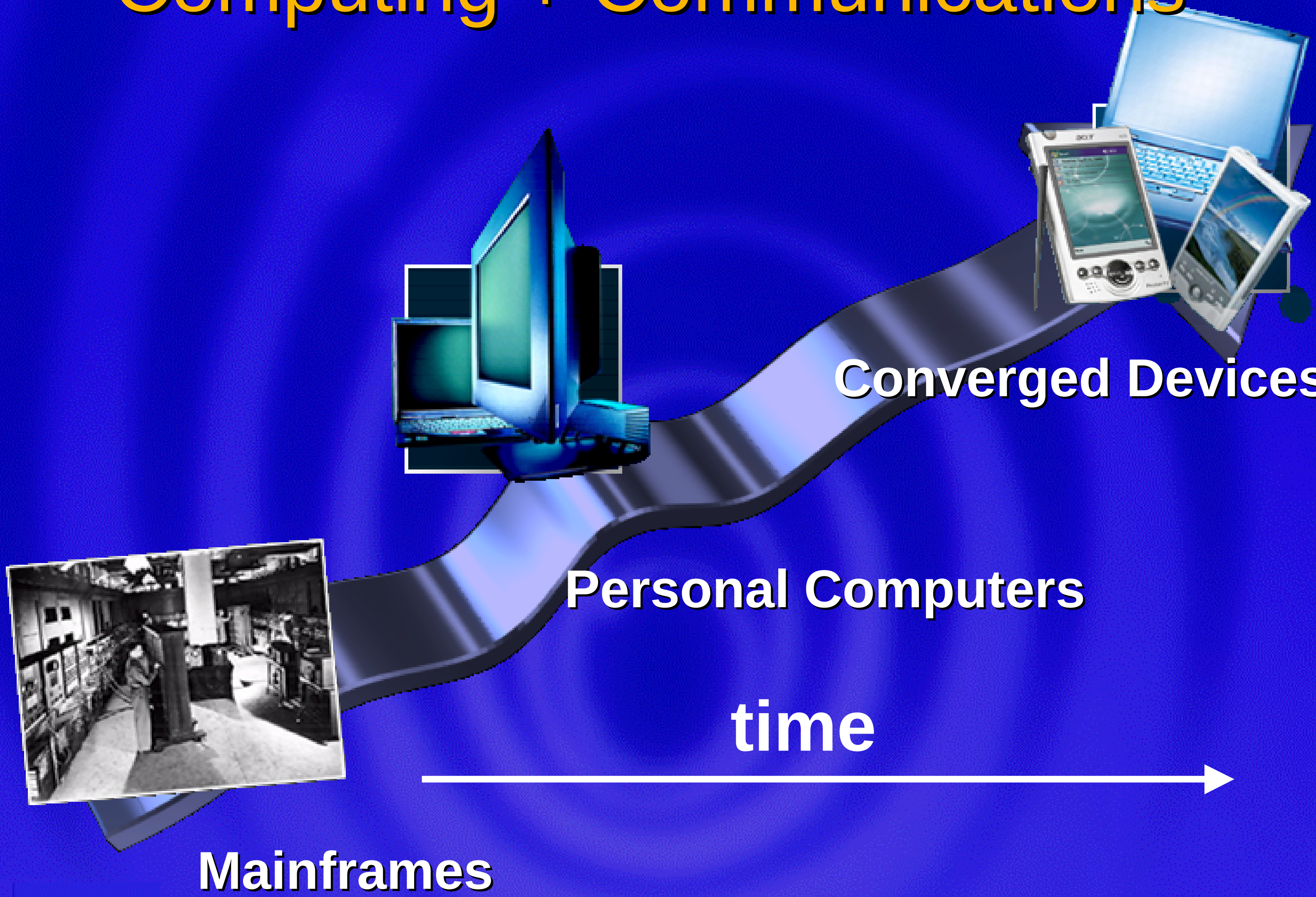
23 November 2002

intel

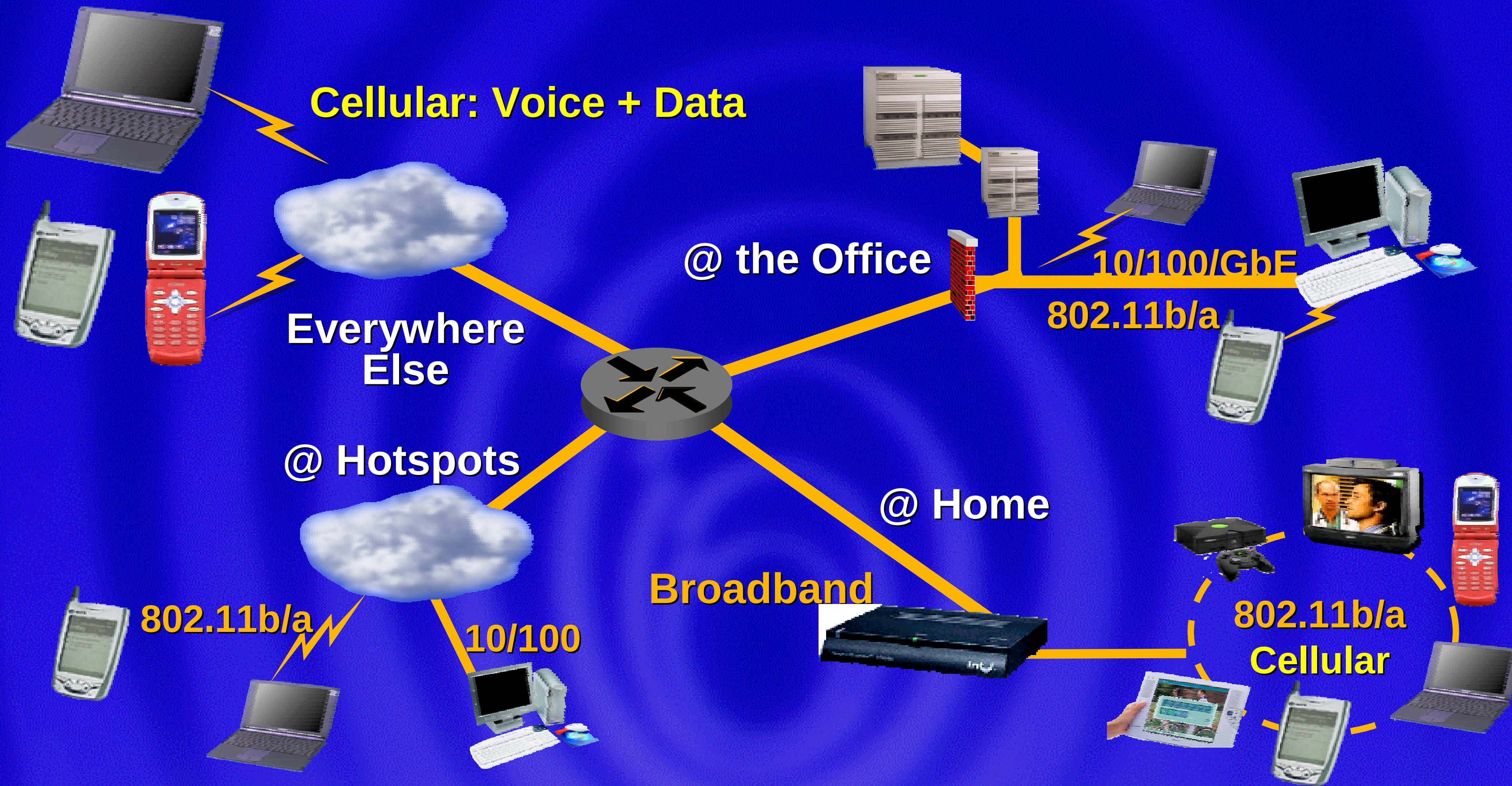
Agenda

- Convergence of computing and communications
- Silicon devices as the integration engine
- Nanotechnology and its impact

Convergence:
Computing + Communications

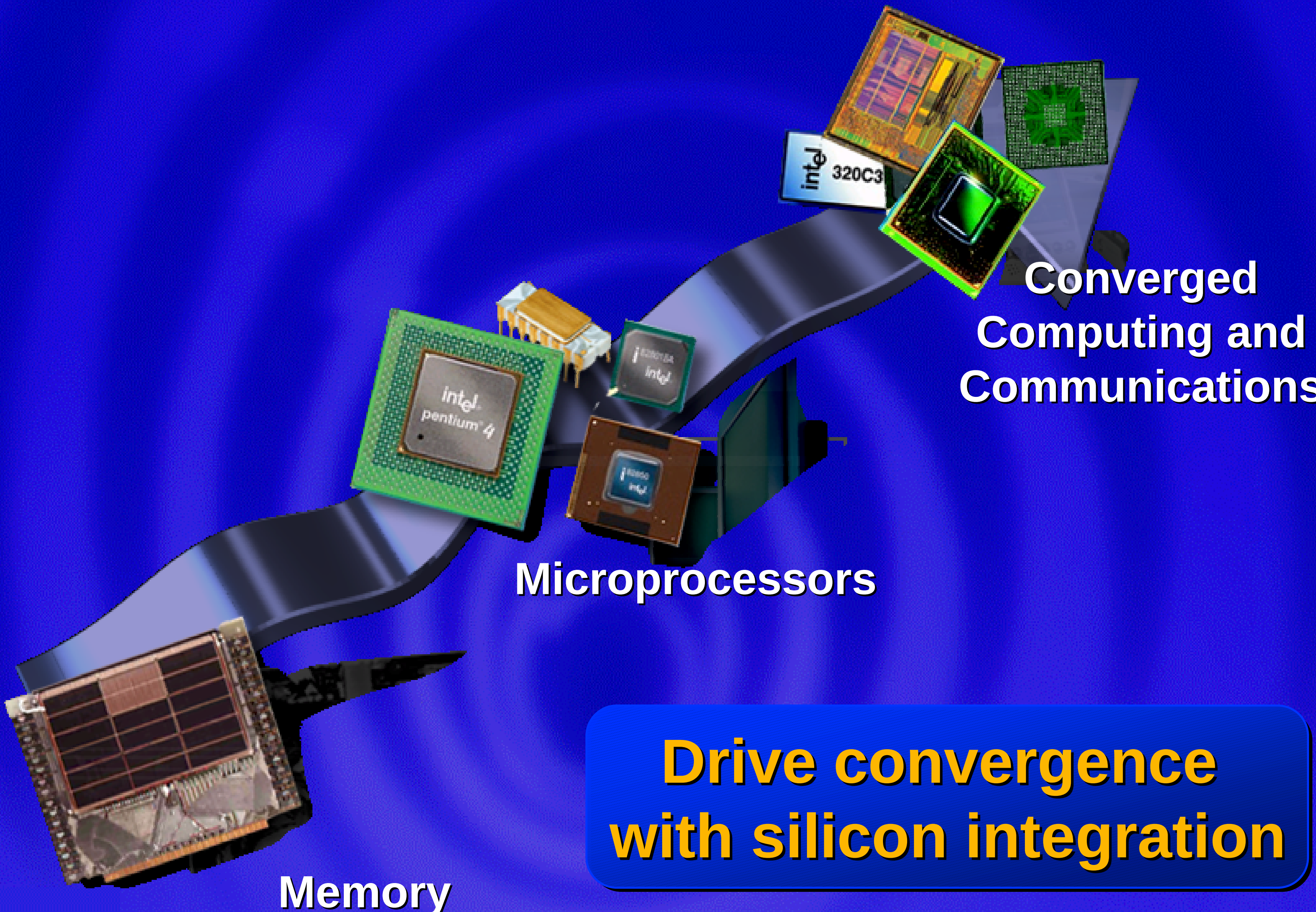


Data Anytime, Anywhere



You are connected

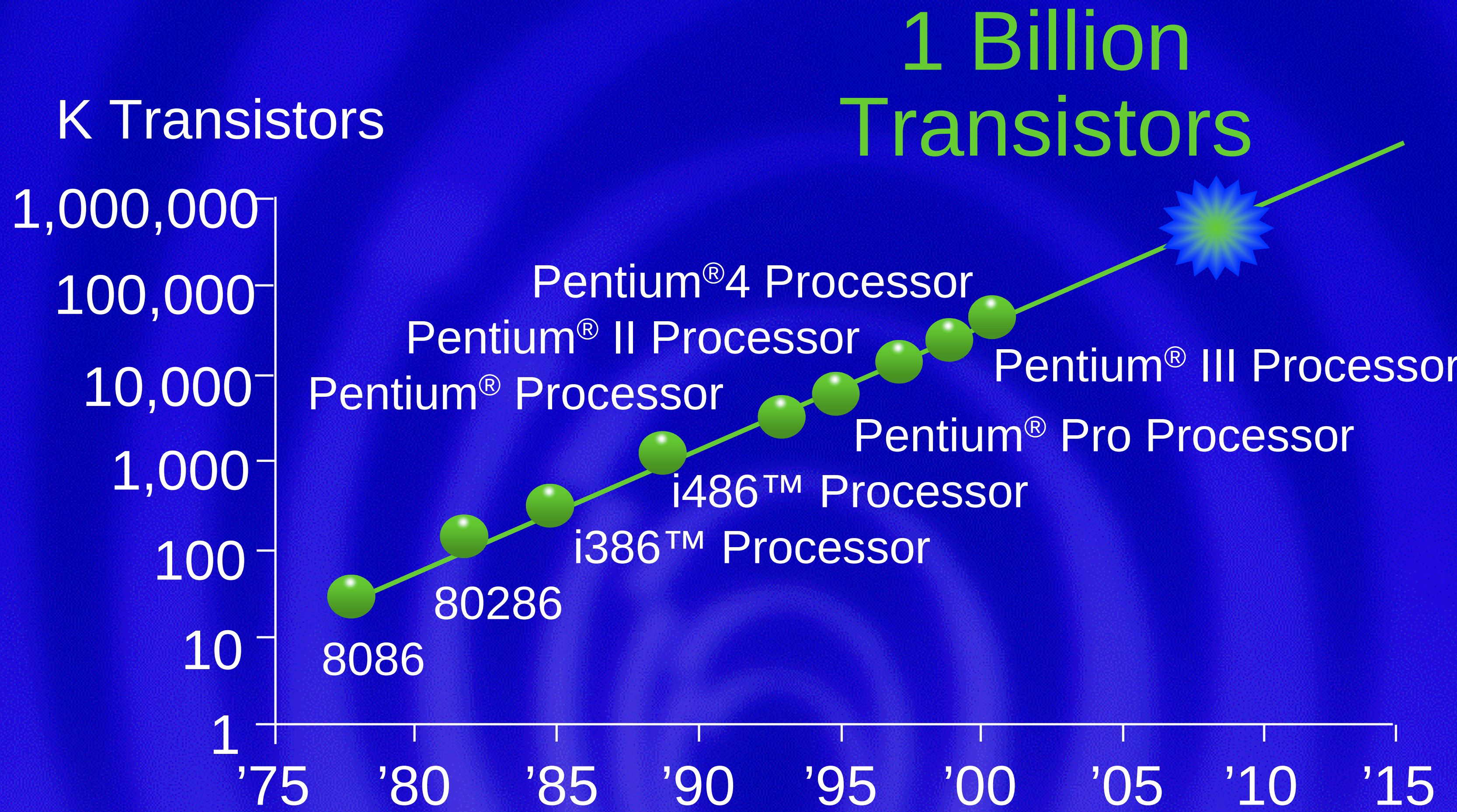
Silicon is the Engine



Drive convergence with silicon integration

Silicon integration makes it possible

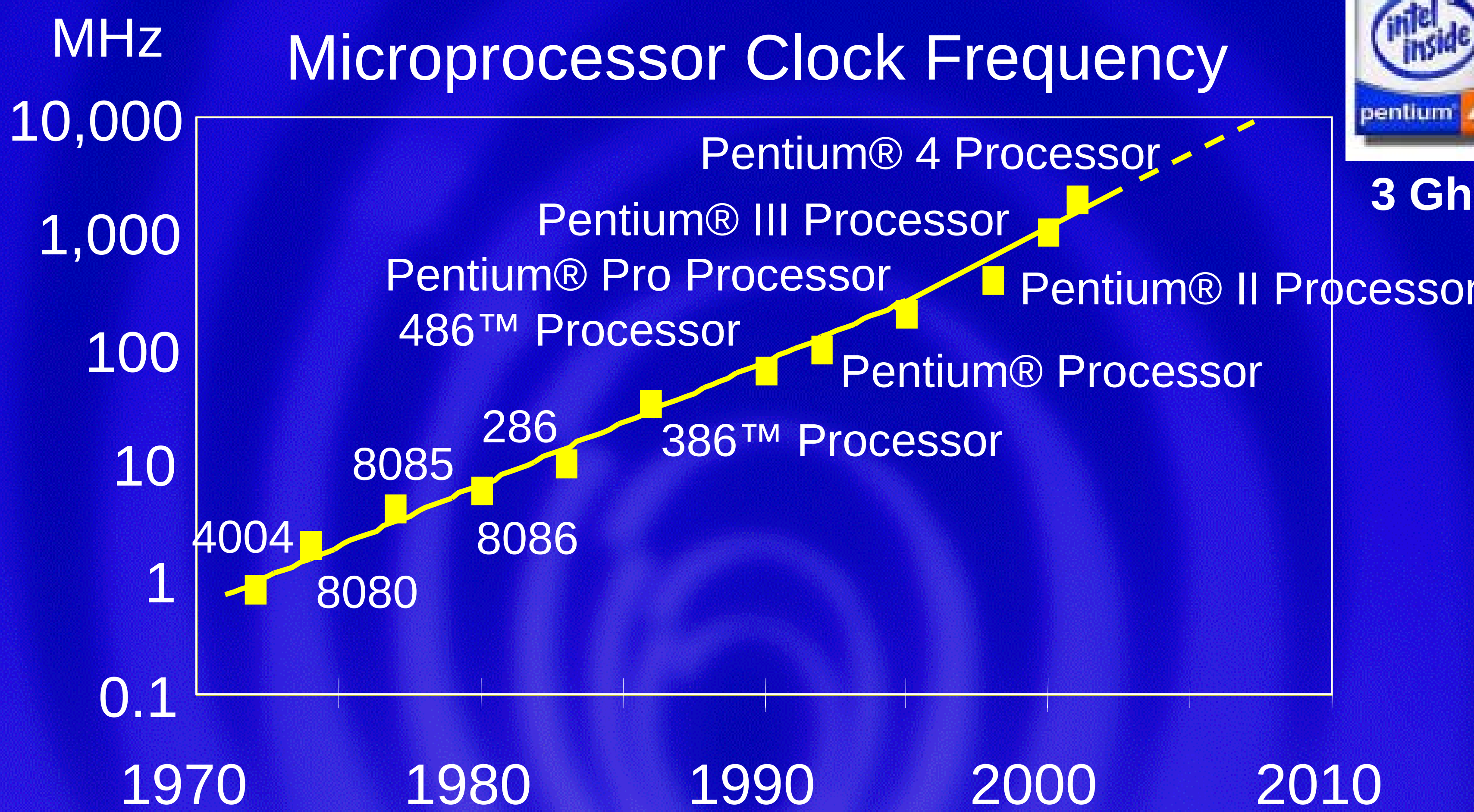
More transistors per chip



Source: Intel

2X every 18 months

Performance increasing



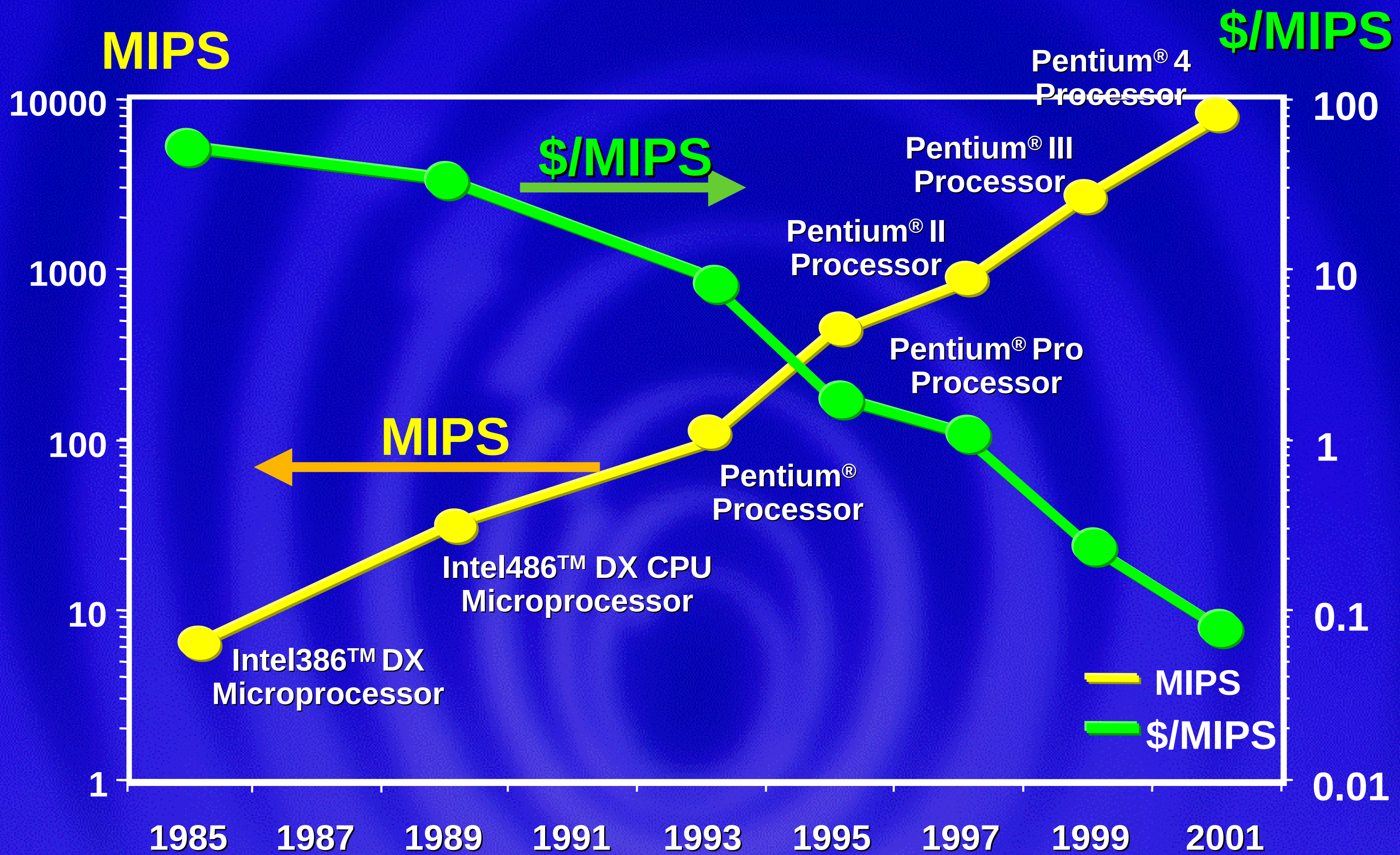
3 Ghz

Source: Intel

2X every 2.5 Yr

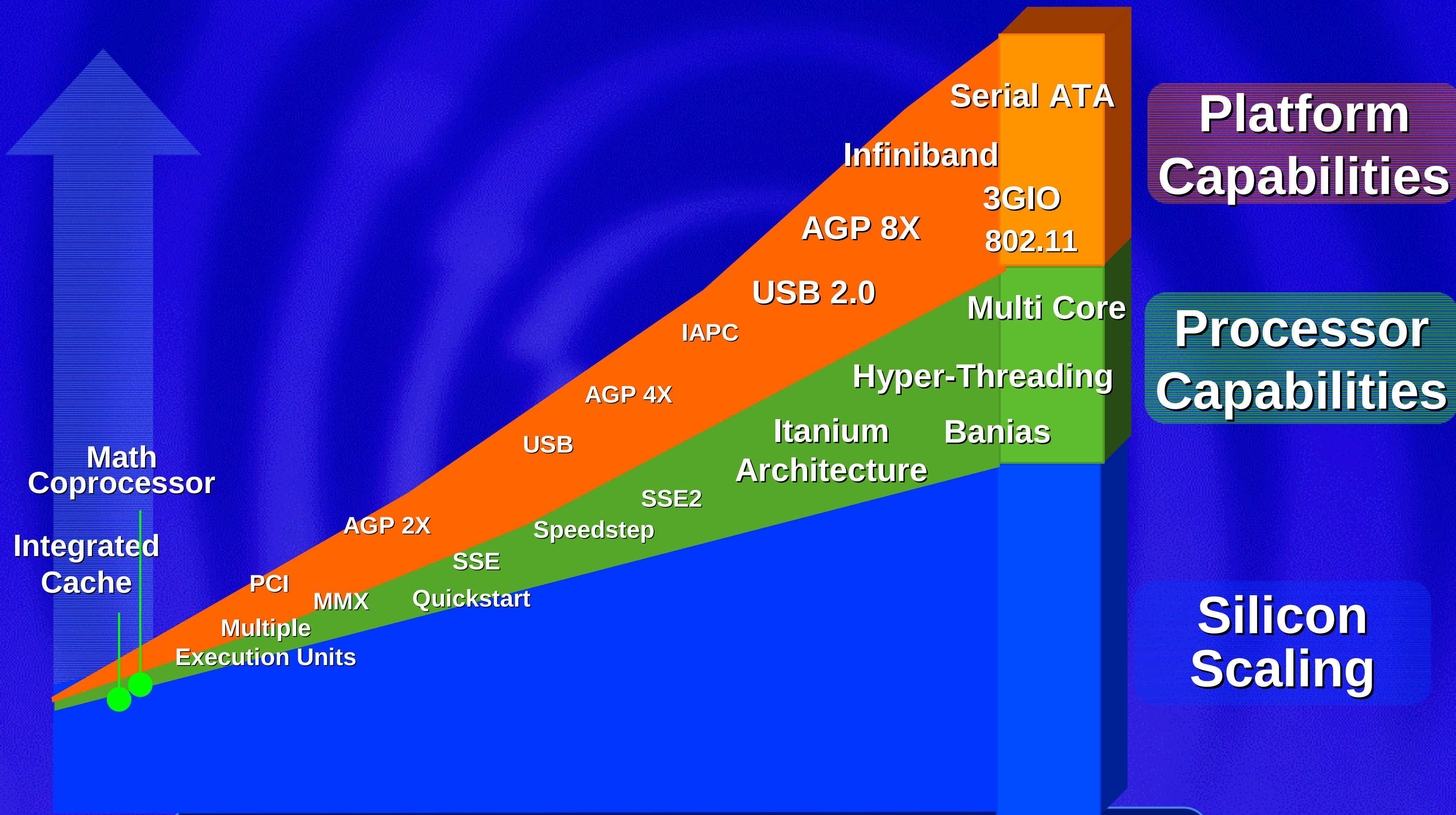
Jose A. Maiz

Higher Performance, Lower Cost



Source: Intel

Architectural Innovations for Enhanced Performance

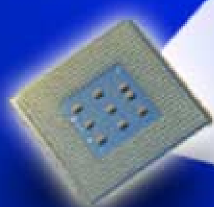


Goal: Usage-relevant performance

Optimizing for Wireless Mobility

Intel's Banias Platform

Promise Was:
CPU

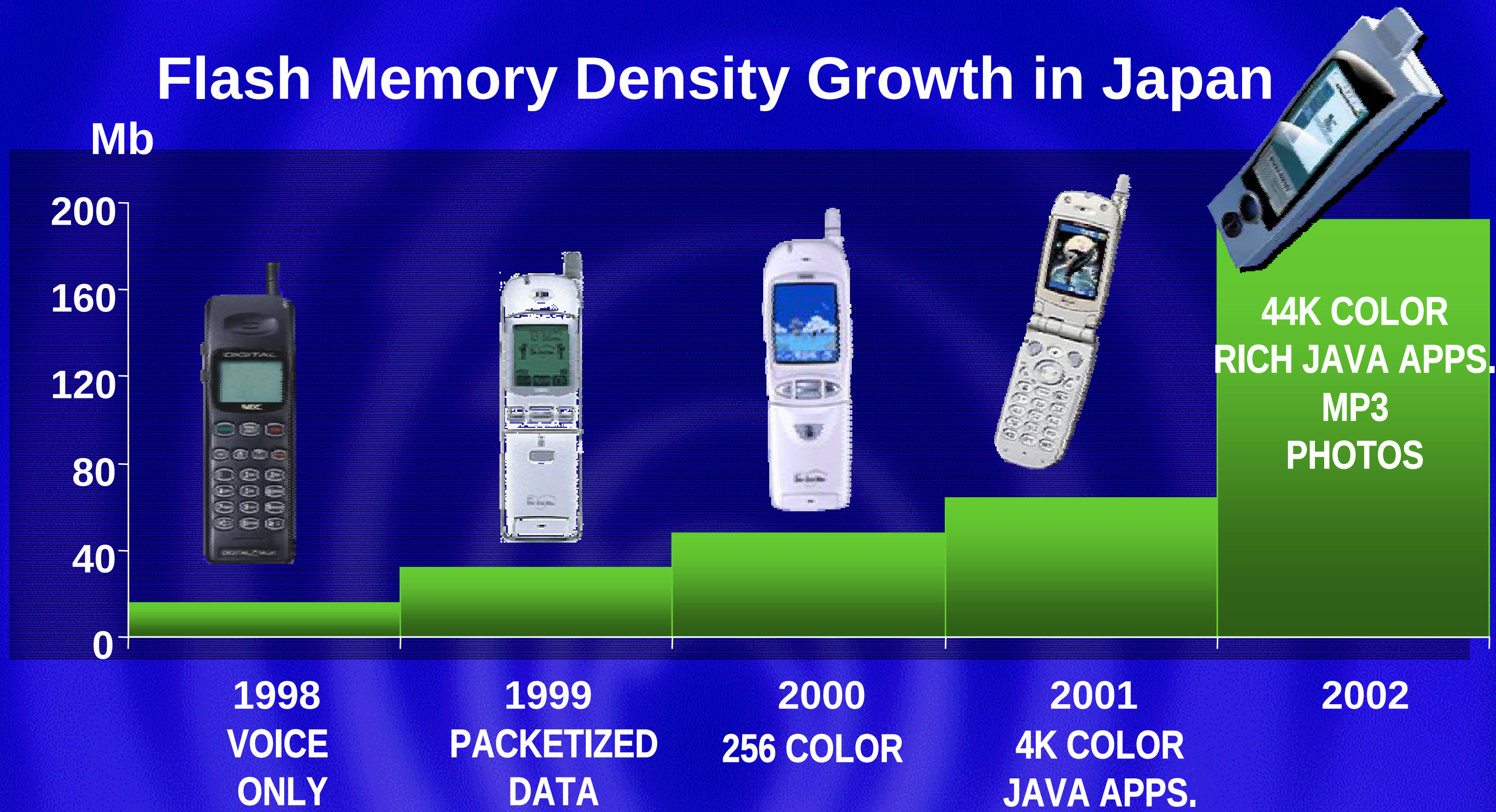


Promise Is:
Fully validated platform delivering mobility

Improved thermals	4. Form factor innovation
Dual-band WLAN	3. Wireless connectivity
Low power	2. Long battery life
Banias CPU performance optimized for low power	1. Performance

MOBILITY

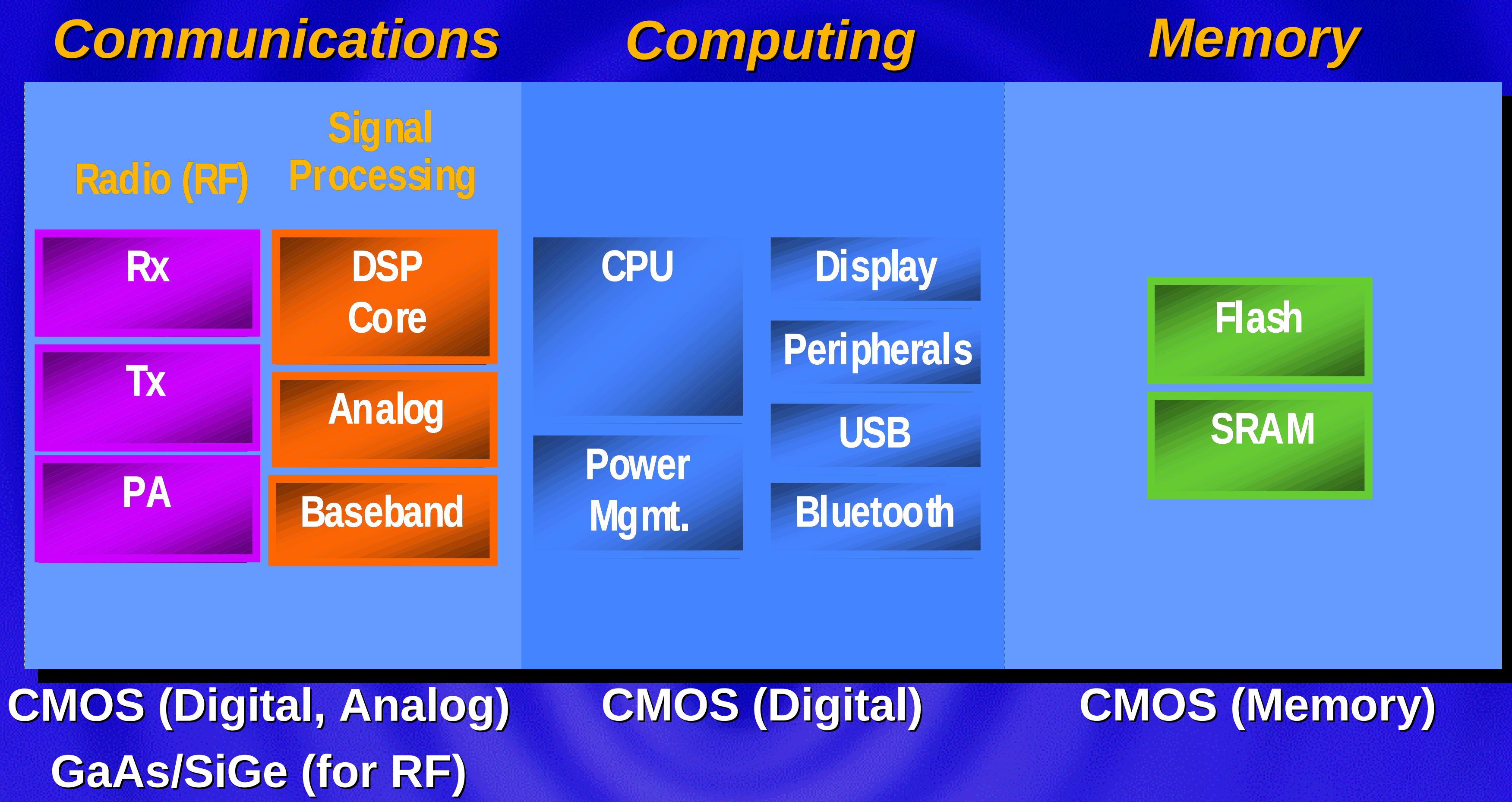
Cell Phones For Voice + Data



Convergence increases silicon usage

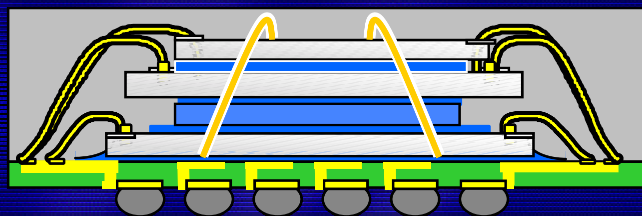
Source: NEC, Intel

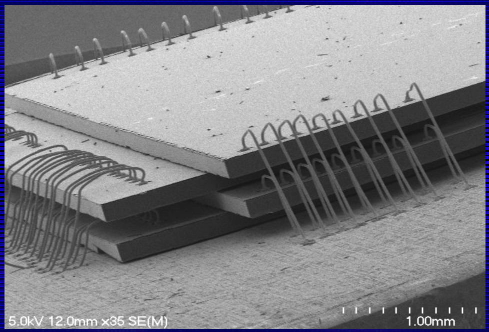
Converged Cell Phone Integration Opportunities

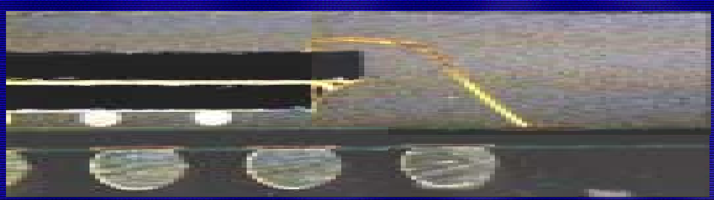


Integration via Packaging

Wirebond Stacked CSP

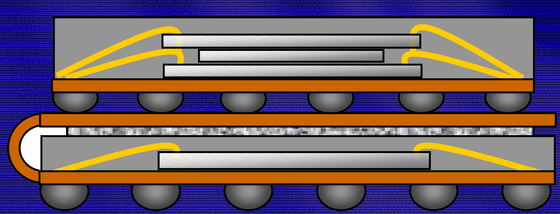


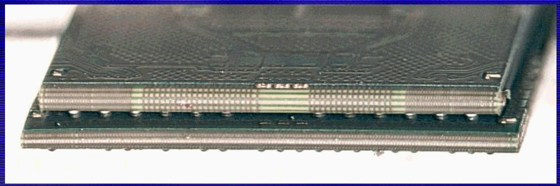




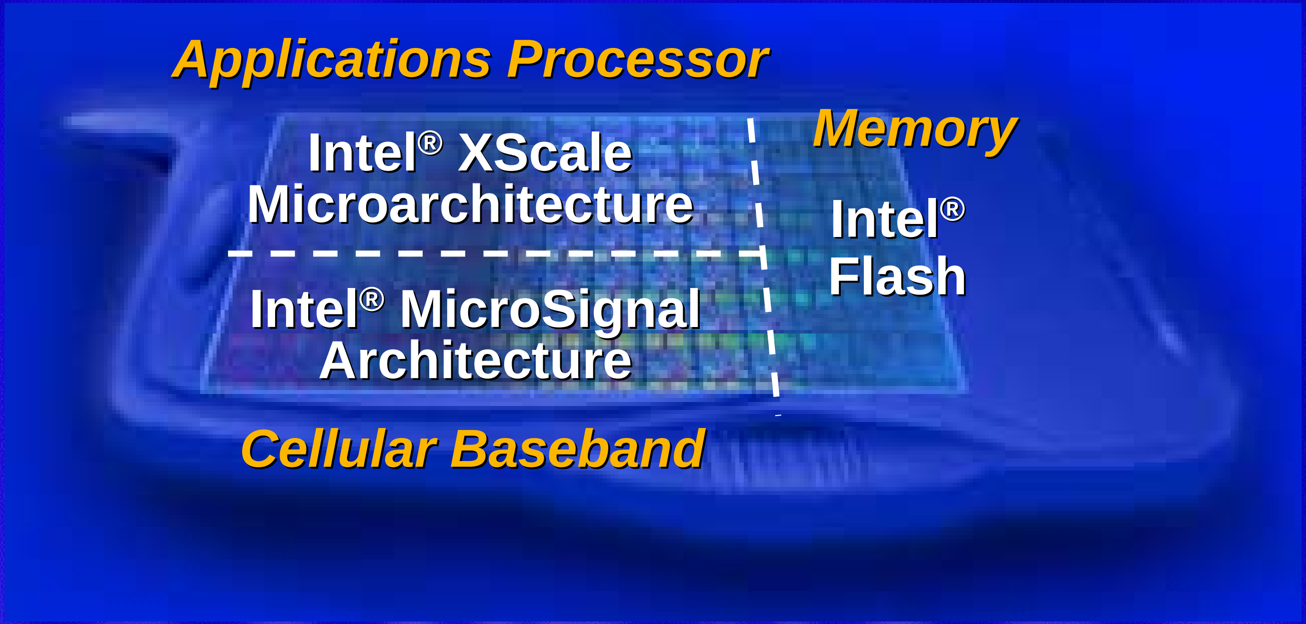
Flip Chip/Wirebond Stacked CSP

Folded Stacked CSP



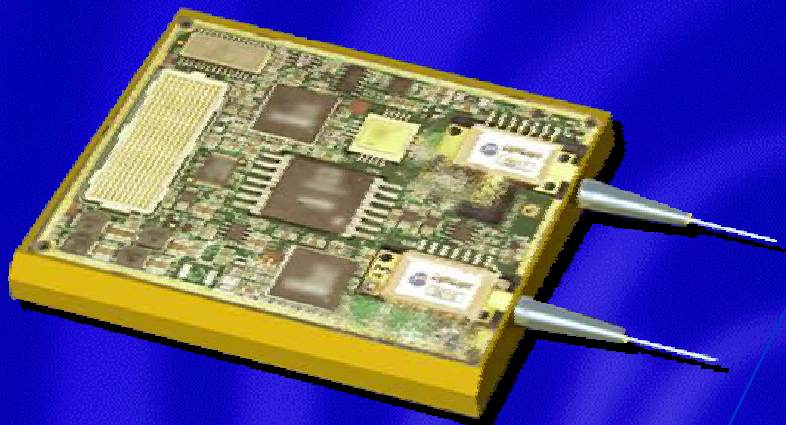


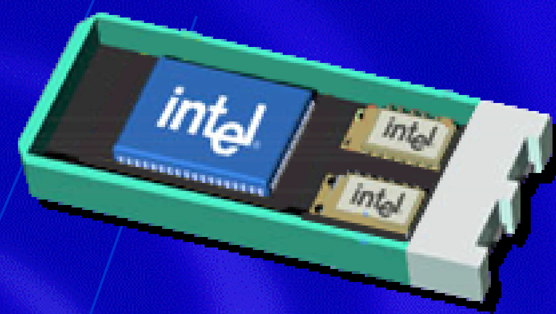
Integration on Silicon Chip



- Total system solution for 2.5G GSM/GPRS products
- Performance headroom for communications protocol stack and data-intensive applications
- Uses Intel's 0.13 micron process technology

Optical Module Integration for Telecom





Today
10+ Chips
4 Process Technologies

Future (90nm)
3 Chips
2 Process Technologies

4x Cost Reduction
3x Power Reduction

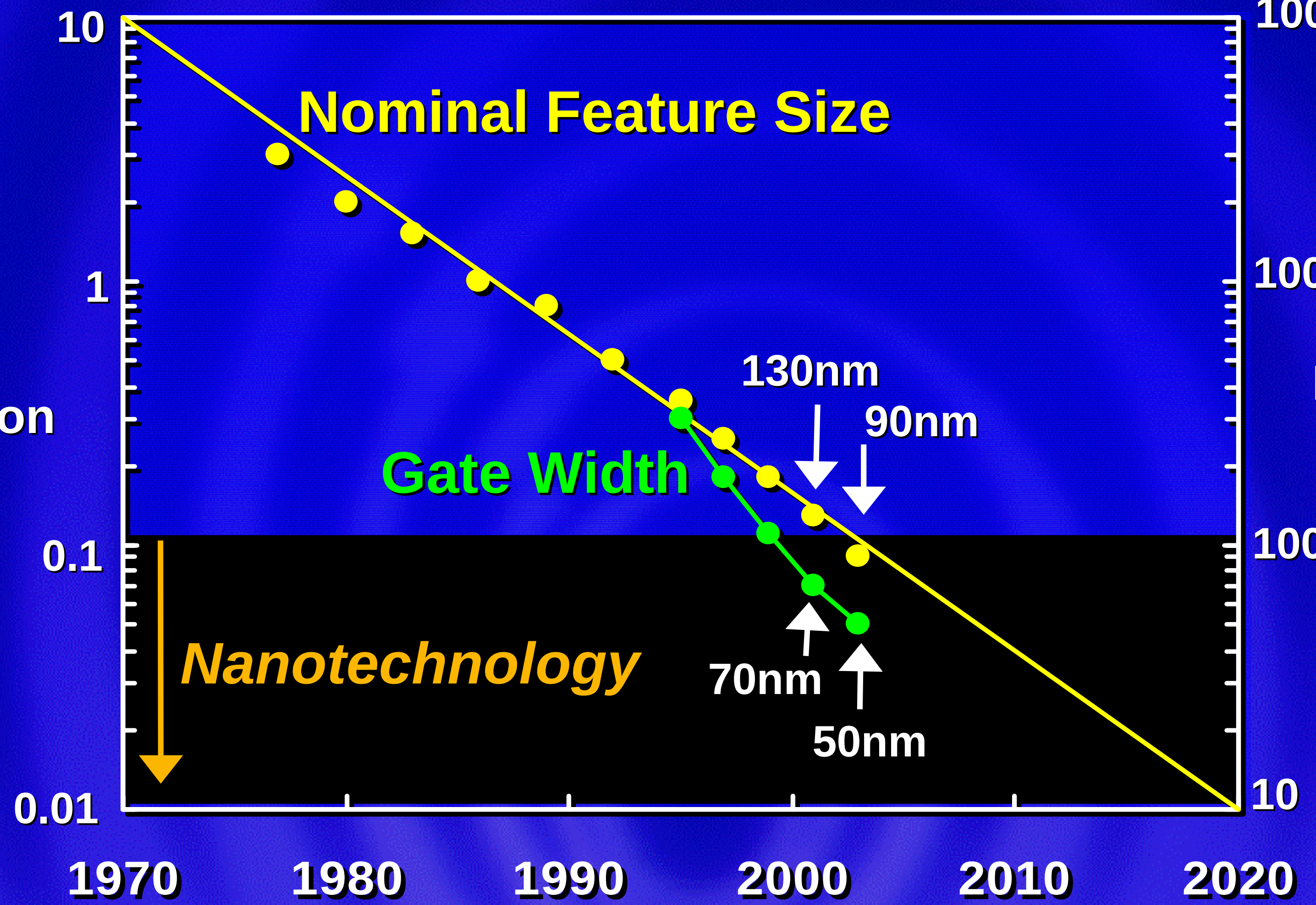
What does it really take

- Aggressive scaling of Silicon technology
- Integration of many new materials
- Convergence of many technologies
- The intersect of nanotechnology

Nanotechnology Features: Challenge & Opportunity

- Structures measured in nanometers
  - Less than 0.1-micron (100nm)
- New materials and device structures
  - Incrementally changing silicon technology base
- Materials manipulated on atomic scale
  - In one or more dimensions
- Increasing use of self-assembly
  - Using chemical properties to form structures

Scaling of transistor dimension

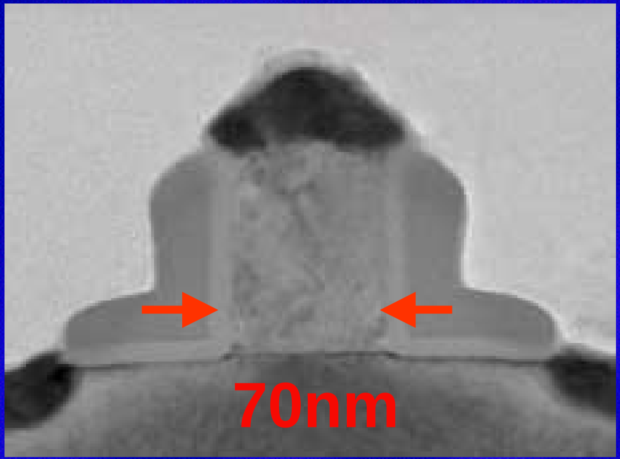


Source: Intel

Shorter gate for increased performance

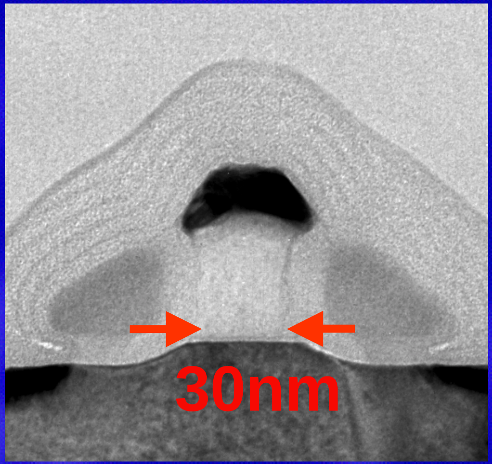
intel

Transistor Scaling

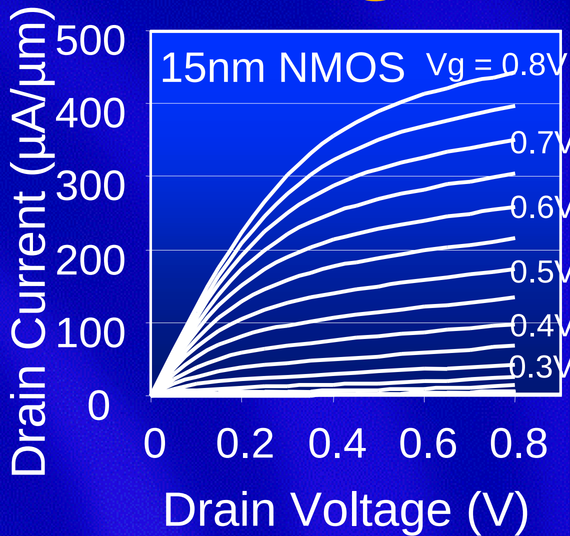


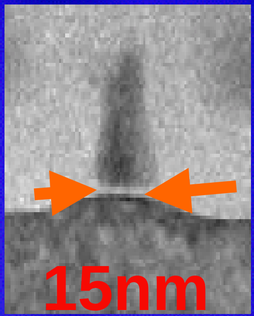
70nm transistor
for 0.13µm process
2001 production

Demo: 2000

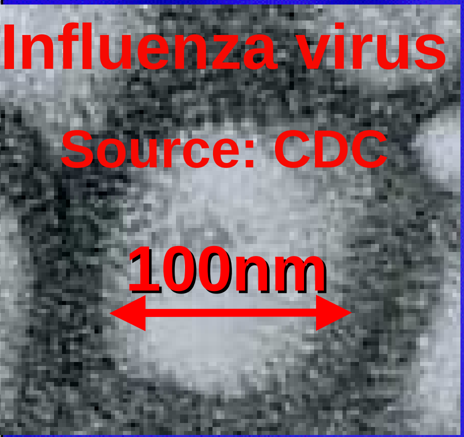


30nm transistor
Prototype



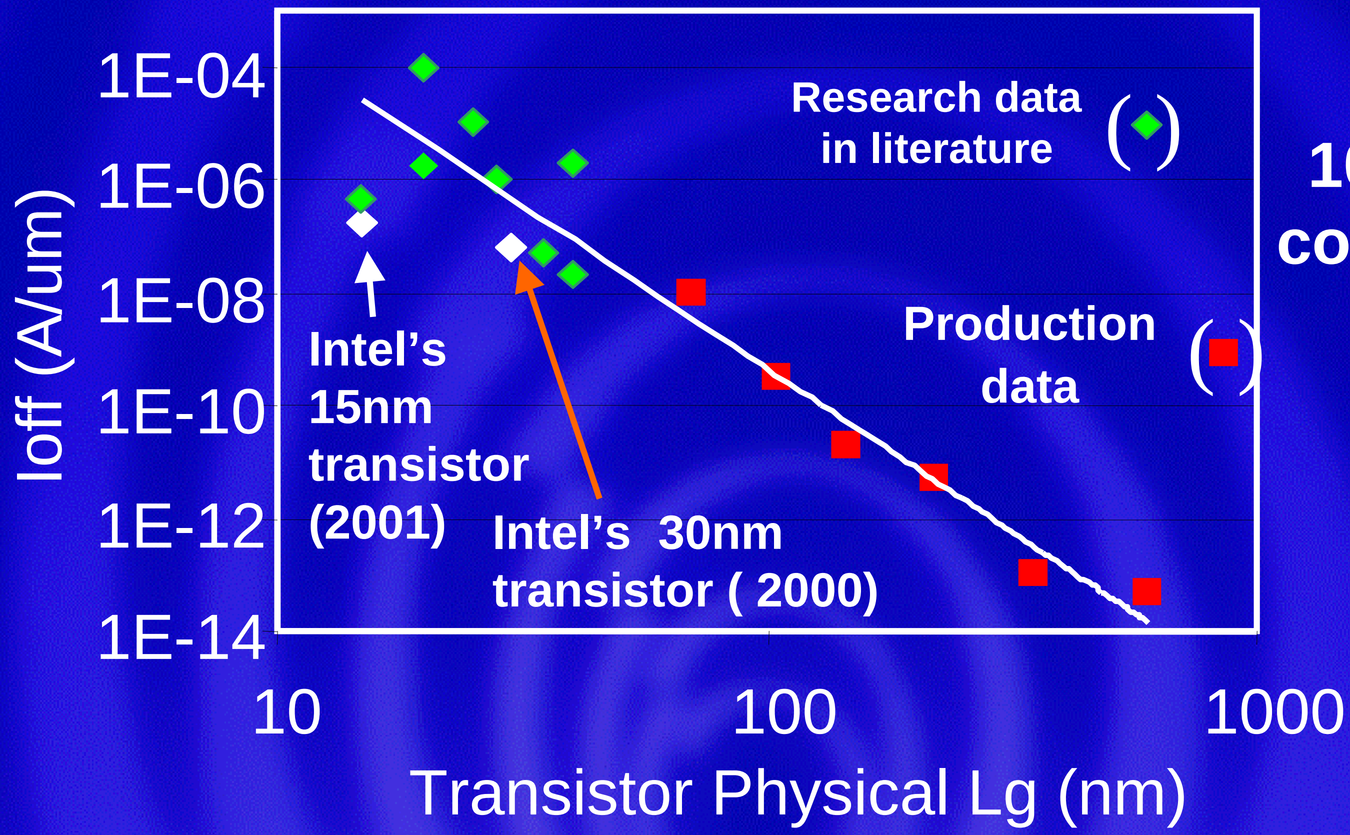


15nm transistor
prototype



Source:
Intel (IEDM, Dec 2001)

The Transistor Problem:
Smaller Devices have Higher Leakage



100A/ 100W components?

Chau et al. 2002 Int. Conf. On Solid State Devices and Materials. Nagoya, Japan

We need novel device structures to meet this challenge

New Materials, Devices Extend Si Transistor Scaling

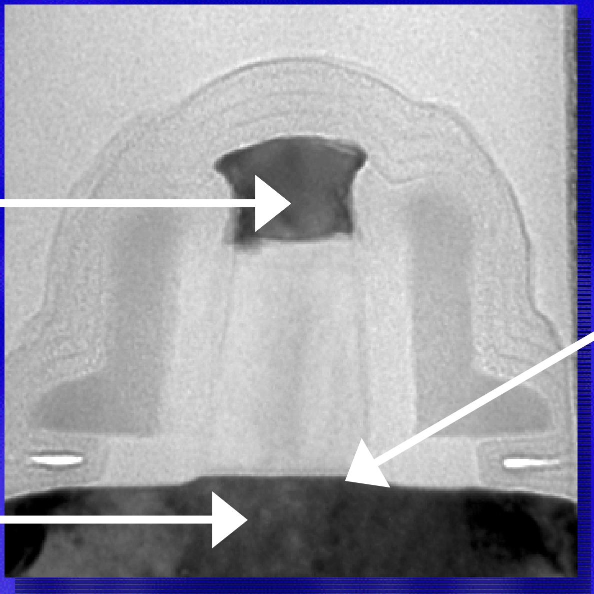
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

Future Options

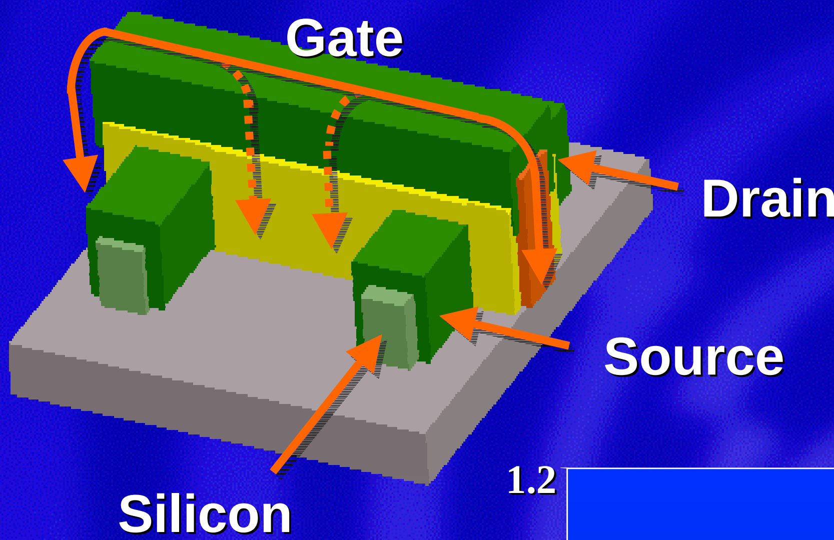
High-k gate dielectric

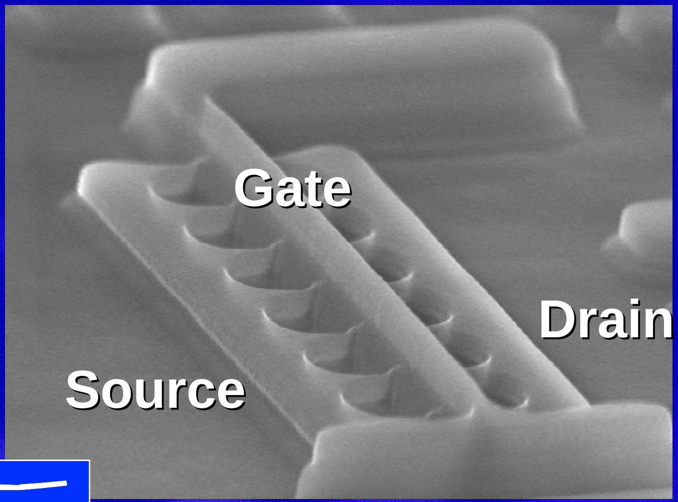
New transistor structure

Source: Intel

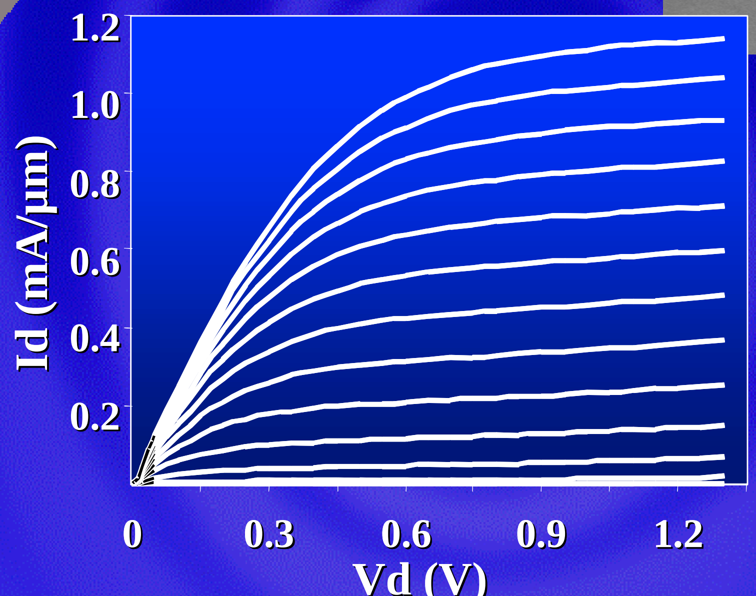
The problem: High Ioff current

Experimental Tri-Gate Transistor Improves Performance, Scalability



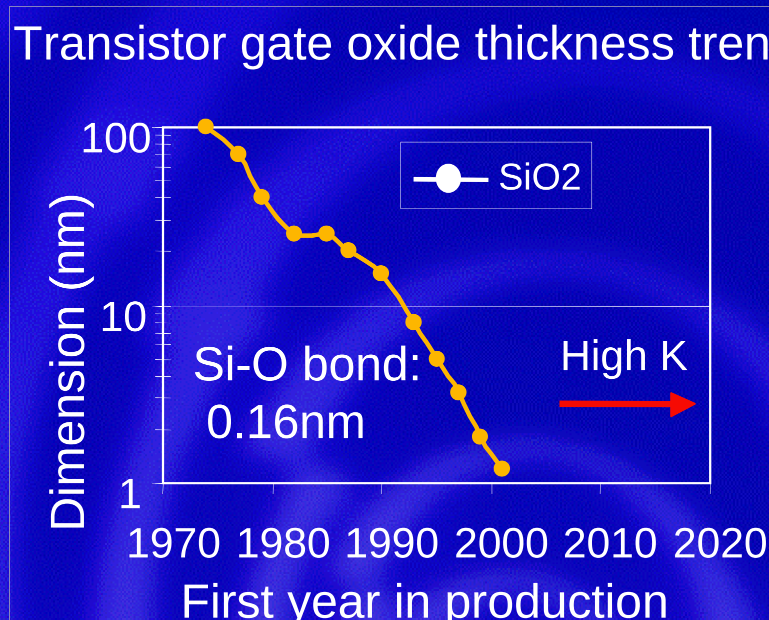


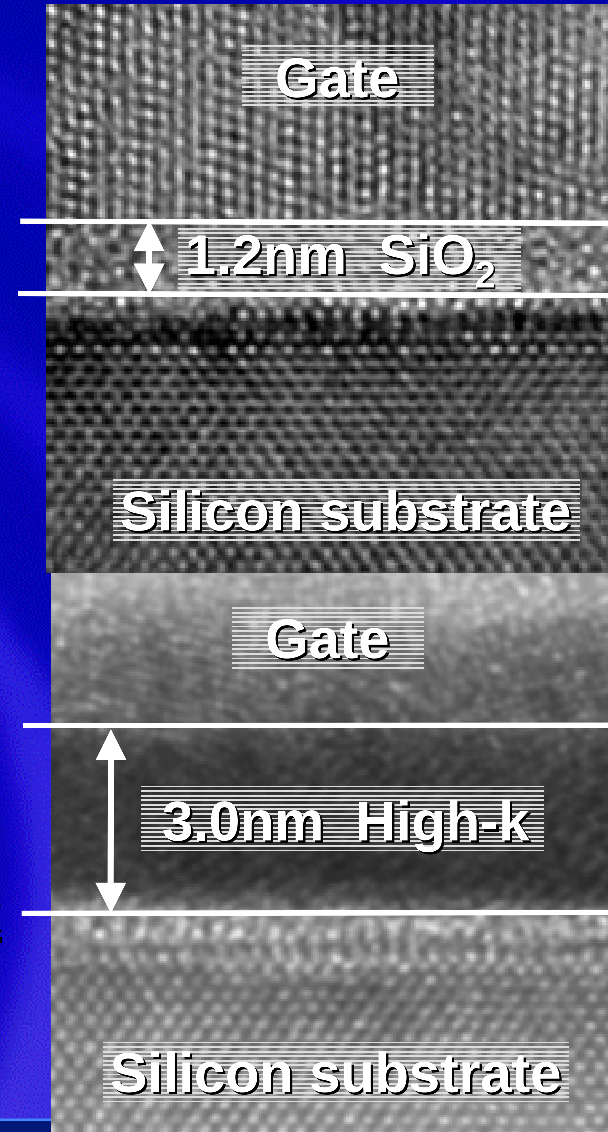
Source: Intel
(ISSDM, Sep 2002)



Source: Intel

Nanotechnology for Gate Dielectrics



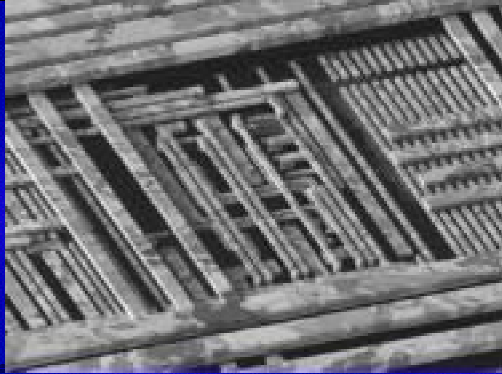


Source: Intel

	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Leakage is the limiter to SiO2 scaling
Integration is the key challenge to High K

New Materials for Interconnects



Changes Made

Metal lines

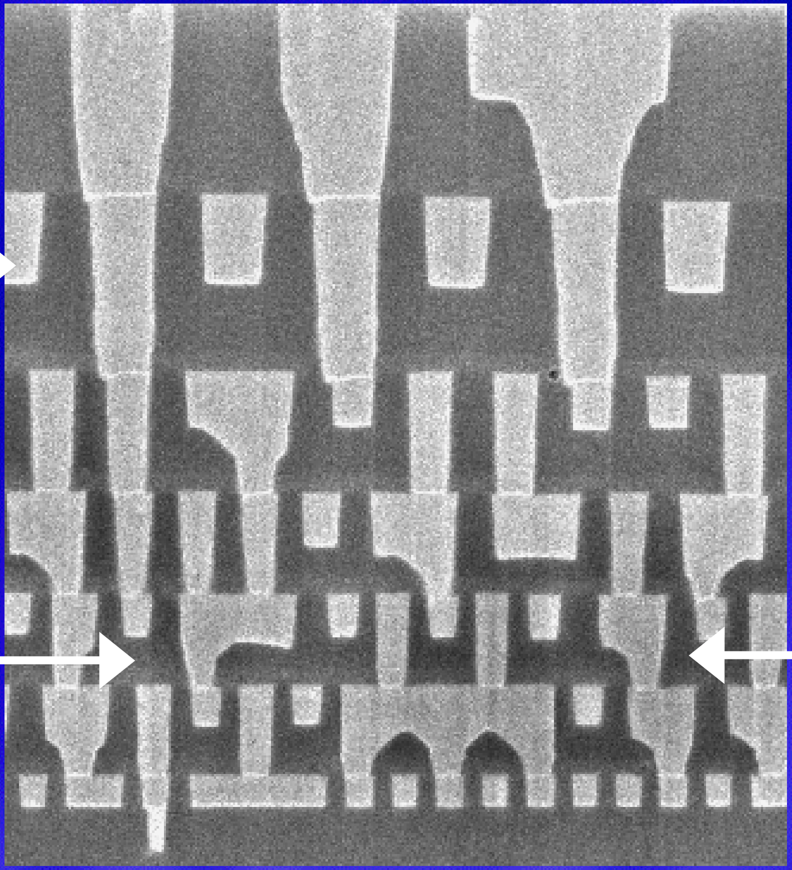
Al → Cu

Insulating dielectric

SiO_2 → SiOF

→ CDO

(low-k)



Interconnects

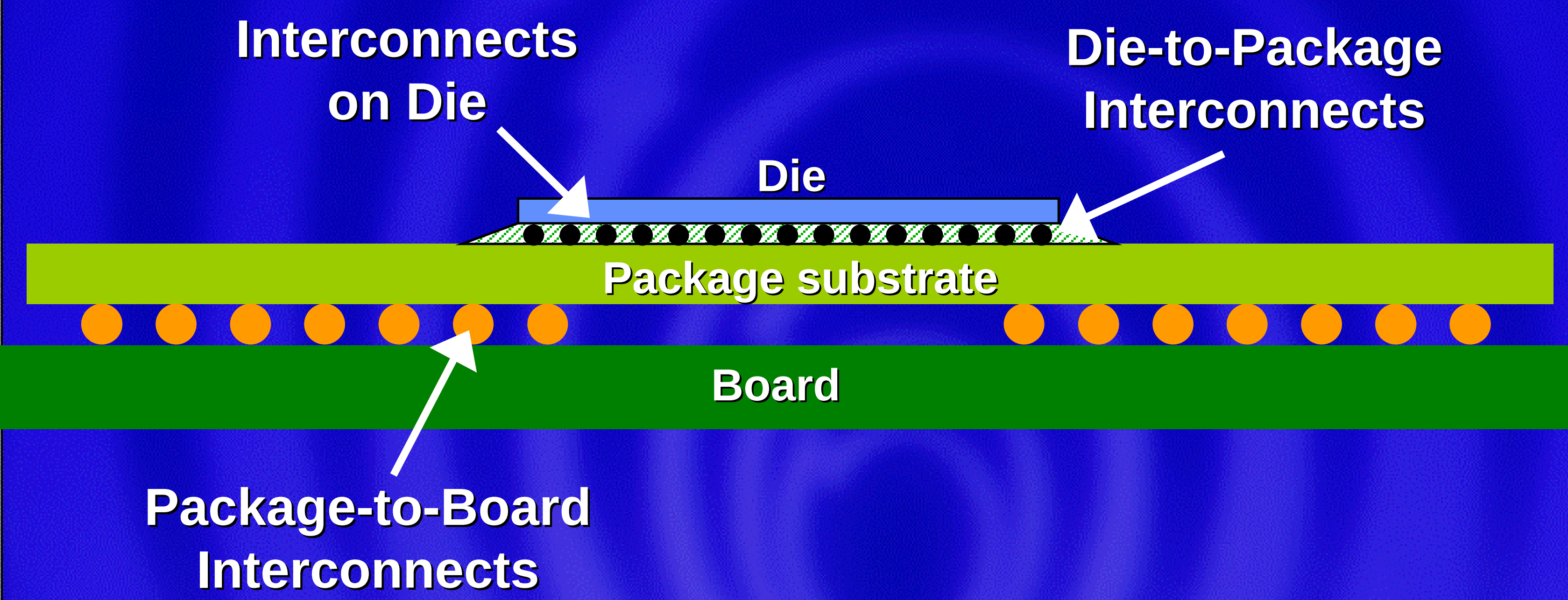
Future Options

Ultra Low-k Dielectric

Source: Intel

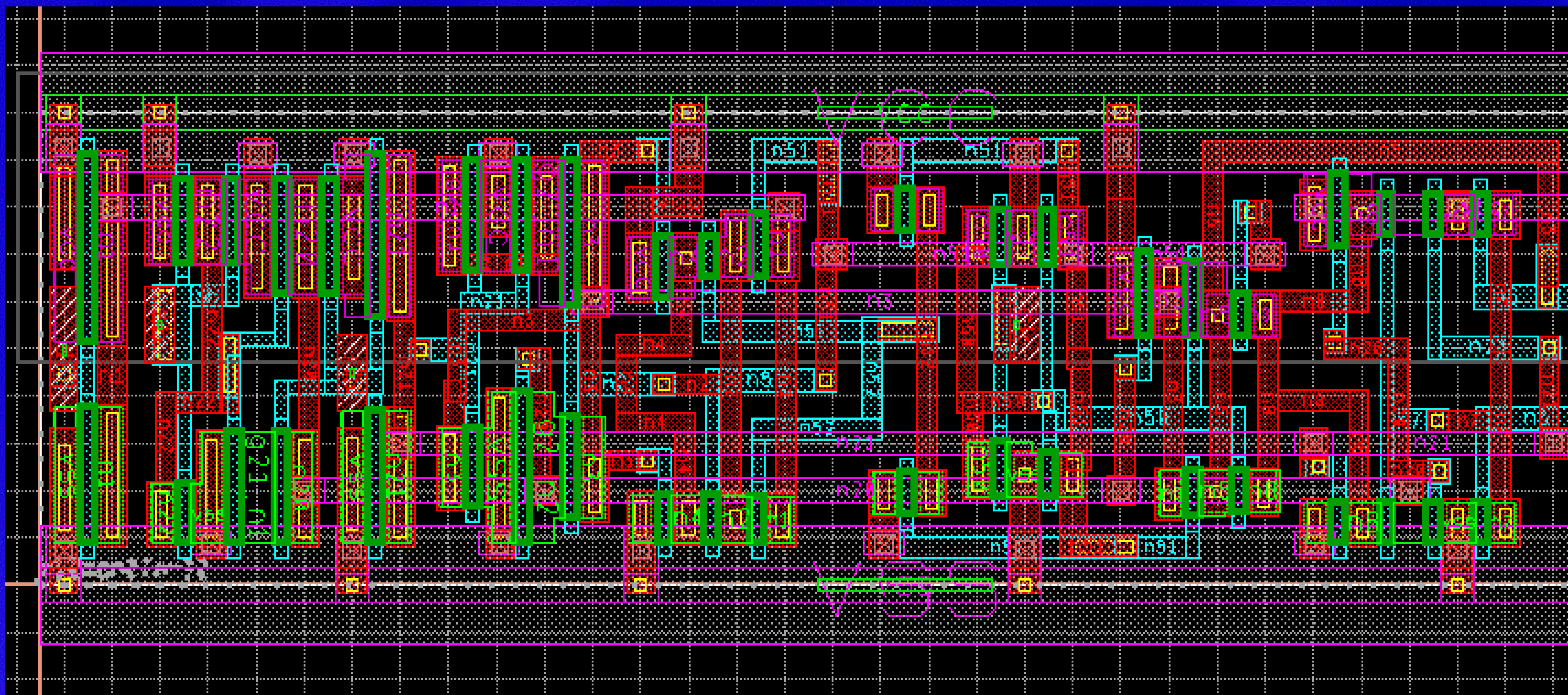
Die / Package Integration More Critical

Points of Vulnerability:



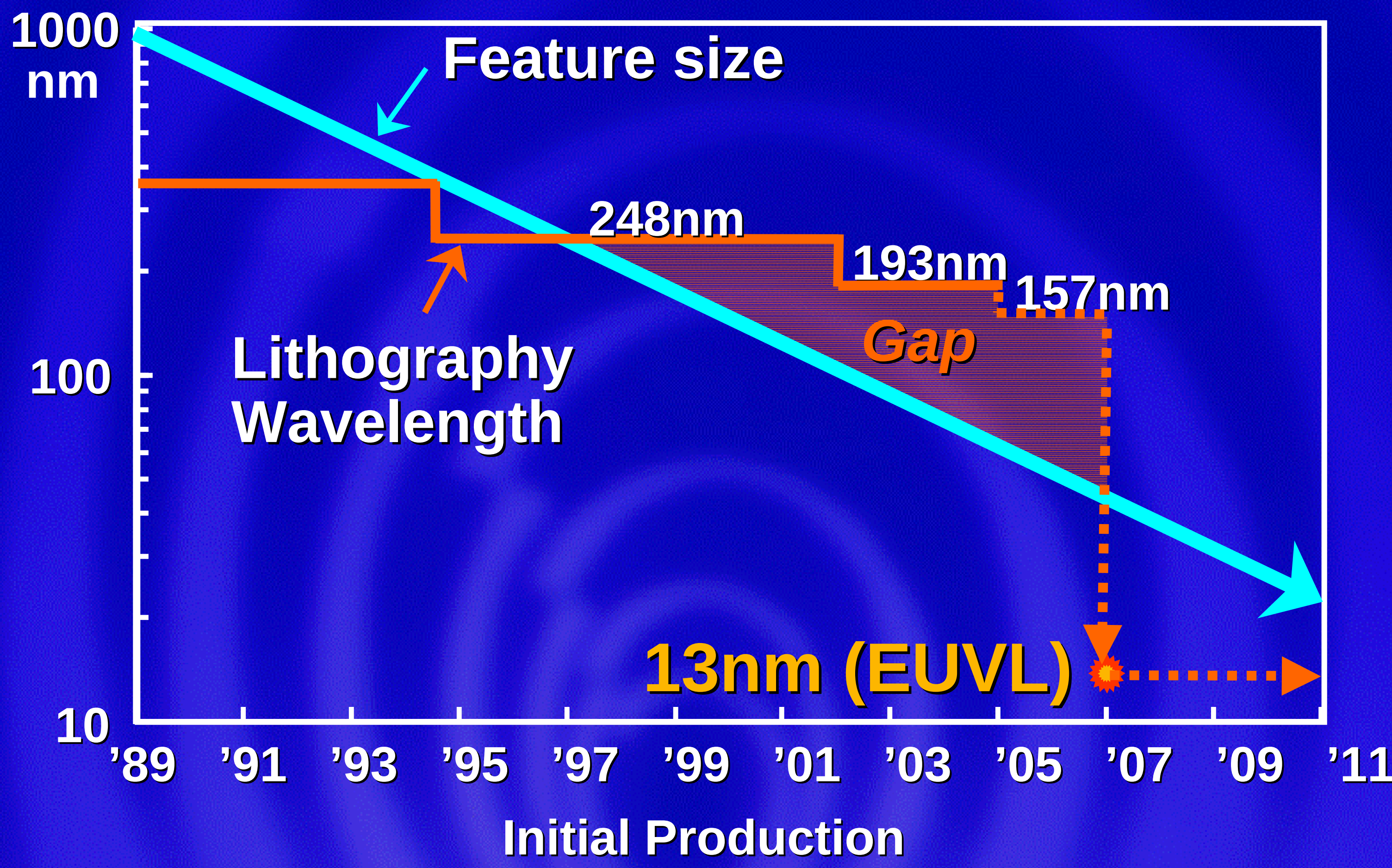
Materials and structures must withstand thermal-mechanical stresses

Lithography Continues to be the Designer's "Brush"



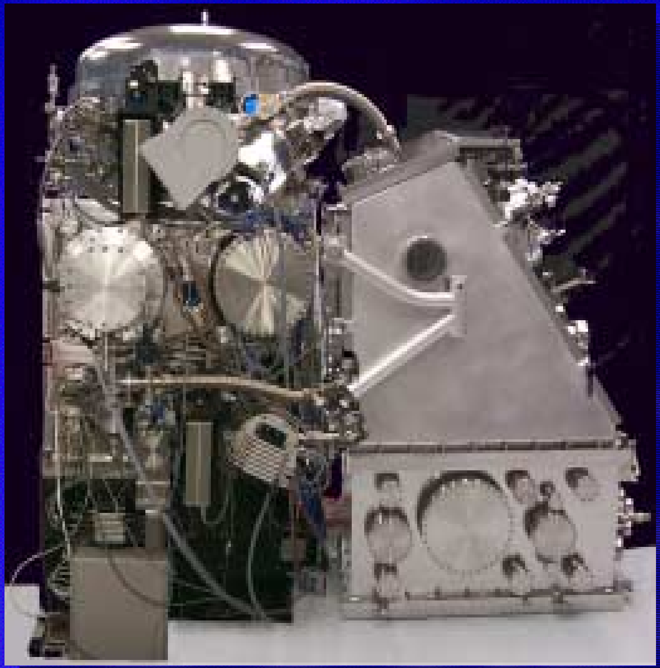
Define locations/configurations of circuit elements/functions

Lithography Challenge

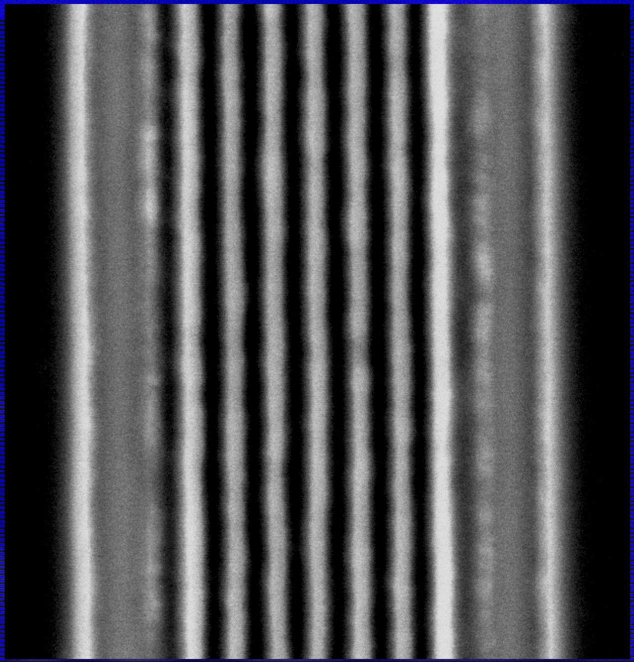


Gap closure with EUV

EUV LLC Consortium Demonstrates EUVL



EUV Lithography Prototype Exposure Tool

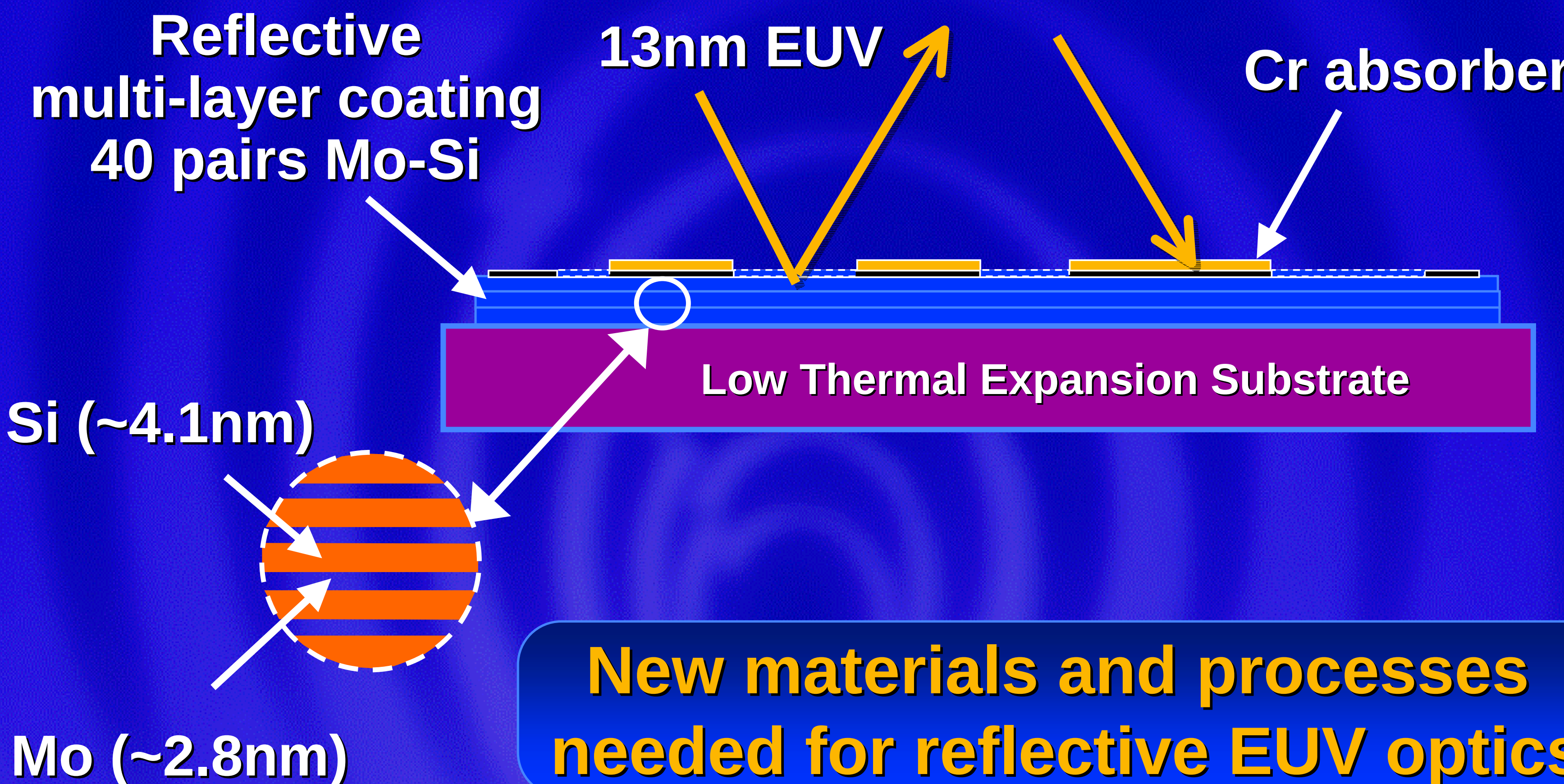


50nm Lines Printed with EUV Lithography

EUV lithography in commercialization phase
Cost effectiveness is key challenge

Source: Sandia

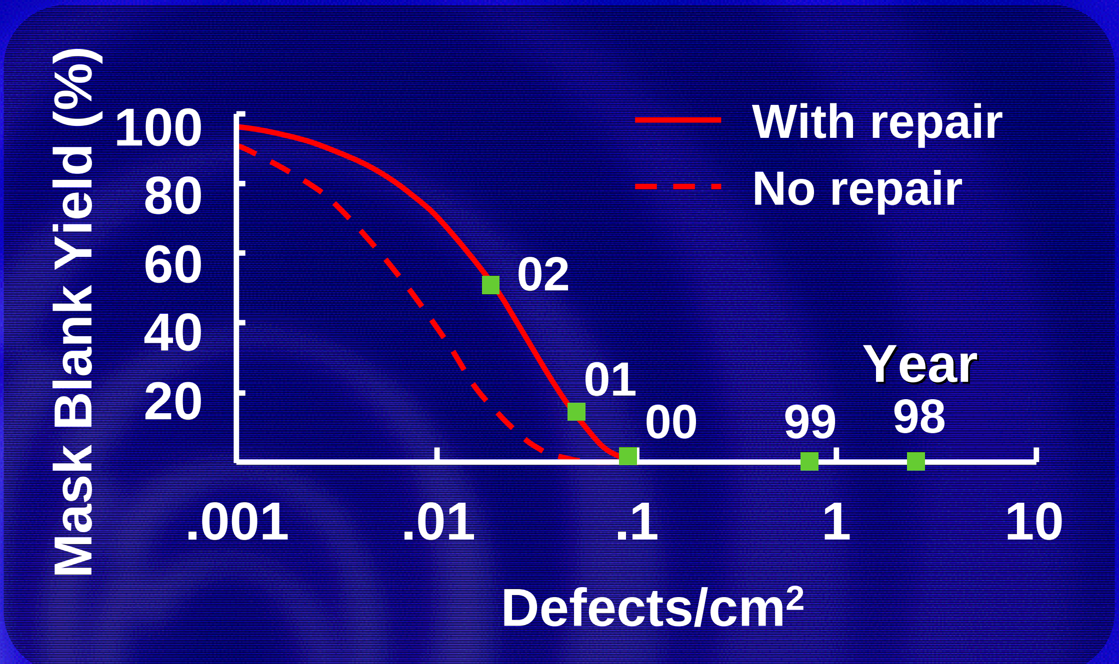
EUV Reflective Mask Structure



New materials and processes needed for reflective EUV optics

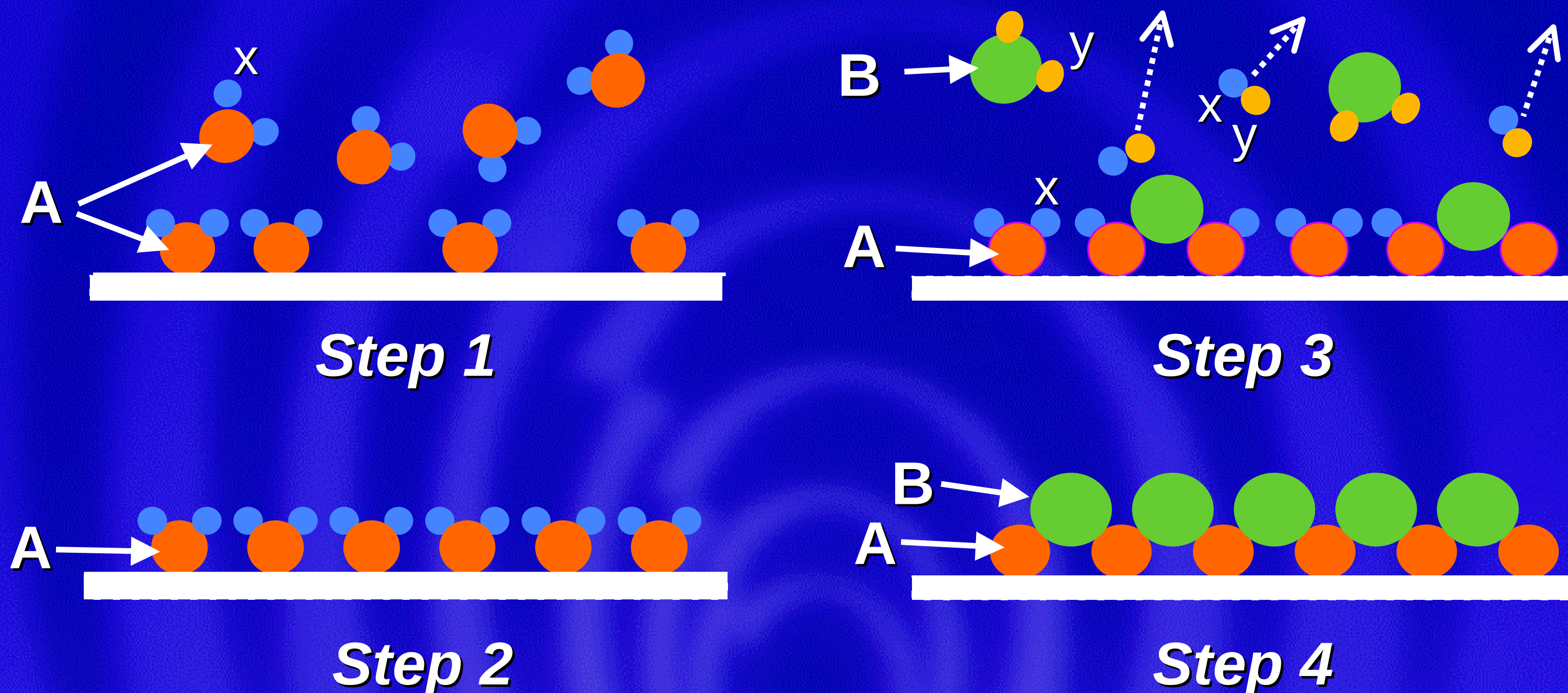
EUV Mask Yield Breakthroughs

EUV Mask



High yield EUV mask fabrication shown feasible

Crafting Films with Atomic Layer Deposition



ALD:
1D Self Assembly nanotechnology in use today

The roadmap

- Scaling of present CMOS technology will continue aggressively until a true limit is uncovered
  - Increasingly complex technology and materials choices
  - Many nanotechnology features
  - Take advantage of the massive silicon infrastructure
  - Complement with new materials/ devices as they get ready
- Component & system architecture will play an increased role in performance improvement and product differentiation
  - Plenty of room for better architectures

Nanotechnology futures

- Many exotic options actively investigated
  - Highly appealing because of the extraordinary properties that they display
  - Large obstacles remain for them to become viable
  - Will likely complement rather than replace Silicon technology

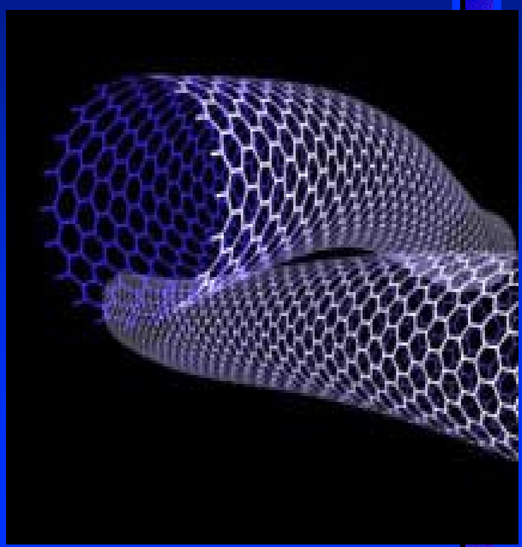
More on the Self Assembly concept

Traditional: Patterning	Self Assembly
• Top-Down approach • Scaling of layers from bulk dimensions • Atomic & molecular granularity is generally an obstacle • Complexity & cost is escalating exponentially	• Bottoms up approach • Self assembly of atoms & molecules into useful structures • Atomic & molecular granularity and distinct properties are an opportunity • Relies on a chemical property or a molecular blueprint for assembly • Living organisms and the brain are superb examples of 3 dimensional, efficient, self assembling, self replicating, high performance, defect tolerant, low power, inexpensive systems

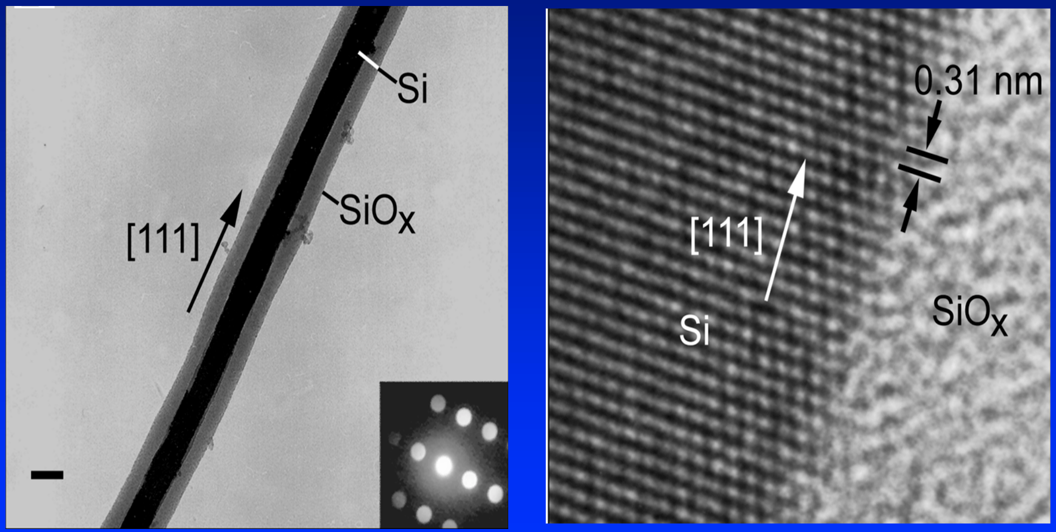
Nanotubes & Nanowires

- Many options including nanotubes/nanowires
- Collaborations with universities in progress

Carbon Nanotube



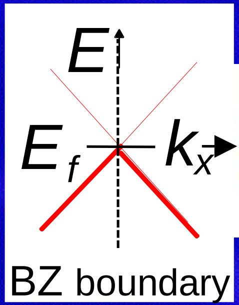
Silicon Nanowire

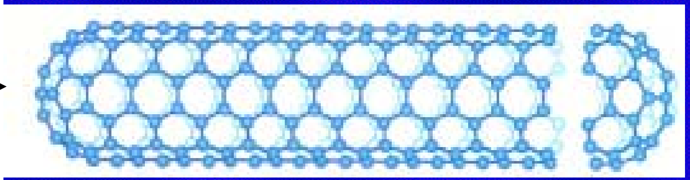


Source: Morales & Lieber, Science **279**, 208 (1998)

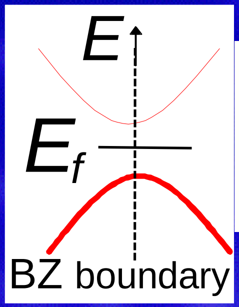
Carbon nanotubes

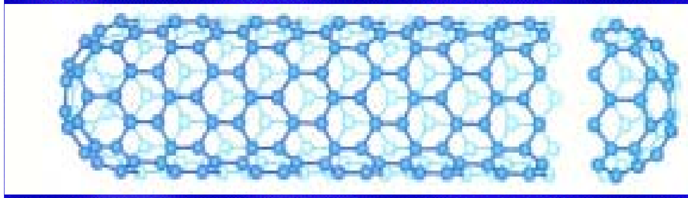
- Self folding of a mono layer sheet of graphite (carbon) into a tube
- Metallic or semiconductor depending on the folding
- Remarkable properties
  - Light, flexible and 100X stronger than steel
  - Thermal conductivity of diamond
  - Electrical conductivity of copper with 1000X maximum current density capability





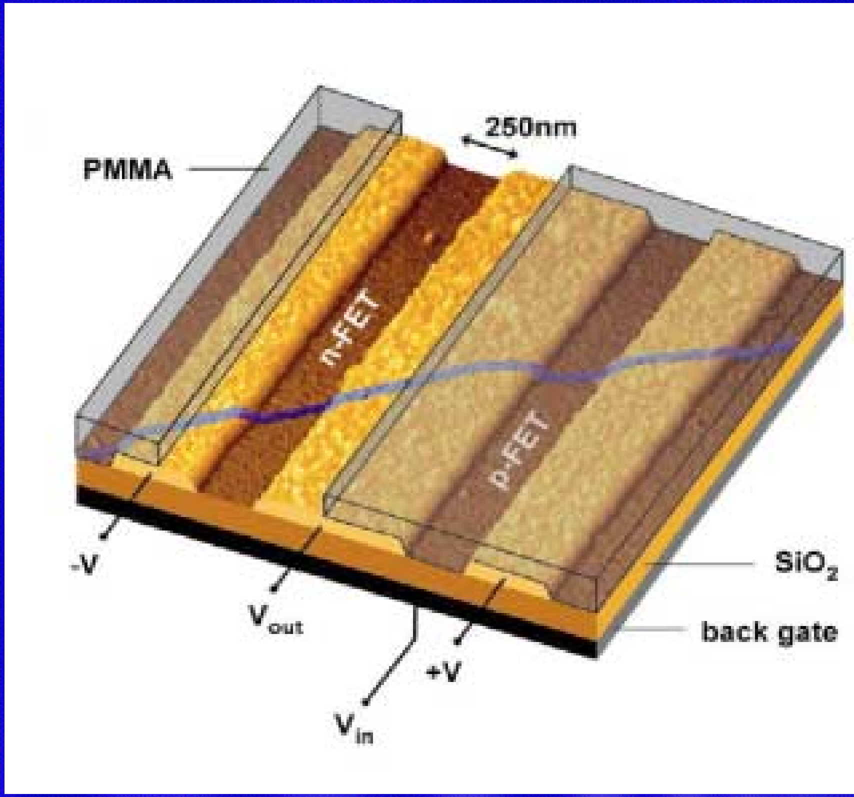
Metallic

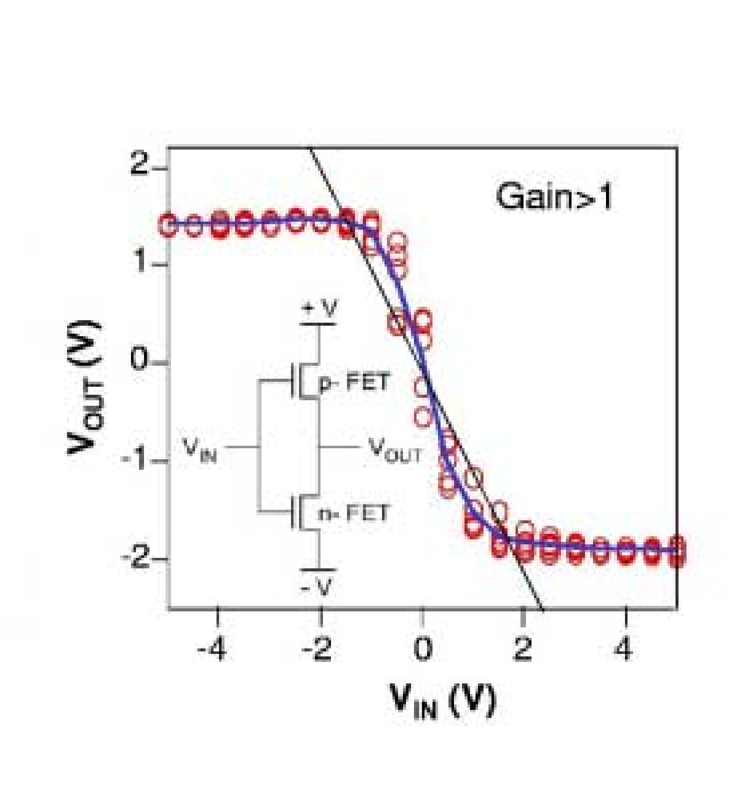




semiconducting

CNT based CMOS inverter demonstrated





Derycke et al. @ www.ibm.com/research

- Inverters and similarly fabricated NOR & NAND gates are the key components of of the most common computer chips

But… Many problems remain

- Chirality (the way the tube folds) is difficult to control
  - Makes control of CNT properties difficult
- CNT assemble and single or multi-walled tubes
- Location, direction and length control necessary for integration into useful devices
- Properties are surface sensitive
  - Contamination, passivation and dopping control will be issues
- Metallic contacts are high resistance
- My guess? 10-20 yr before they make any significant impact

Molecular transistors
An example

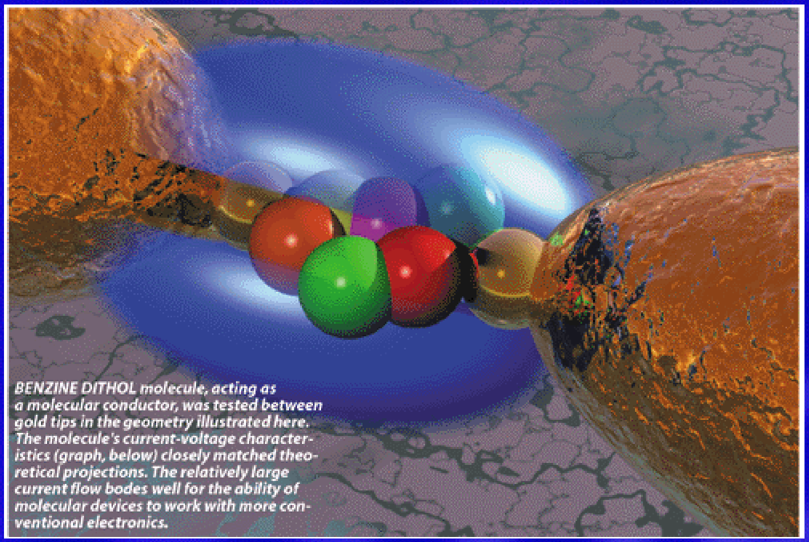
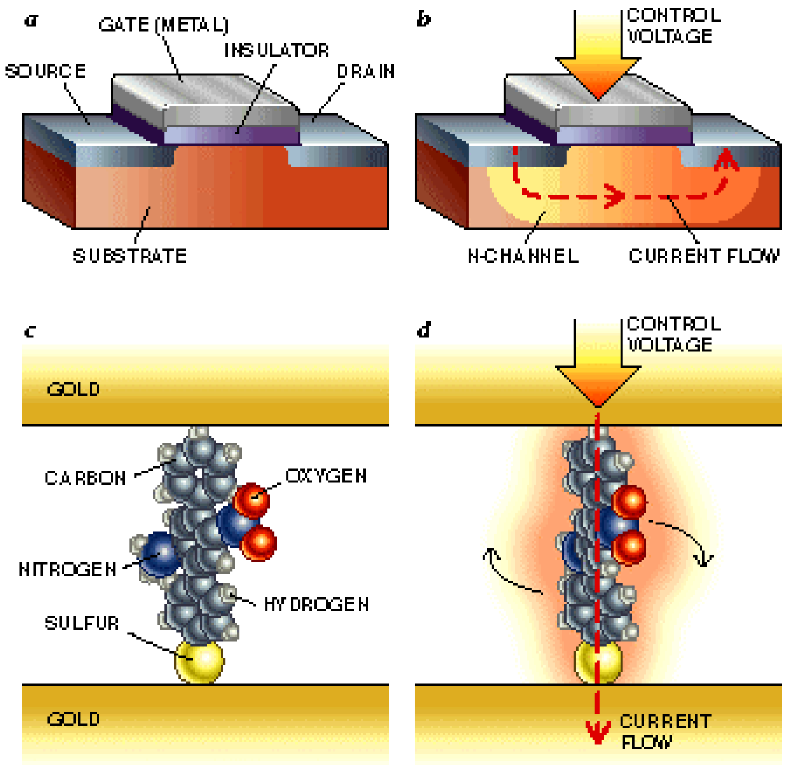


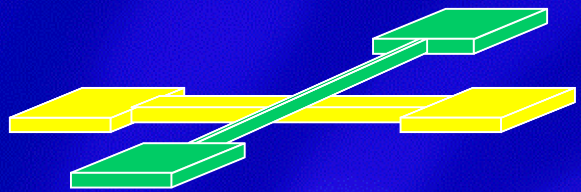
Illustration: Jared Schneidman
See M. Reed et al. @ Scientific American, June 1999

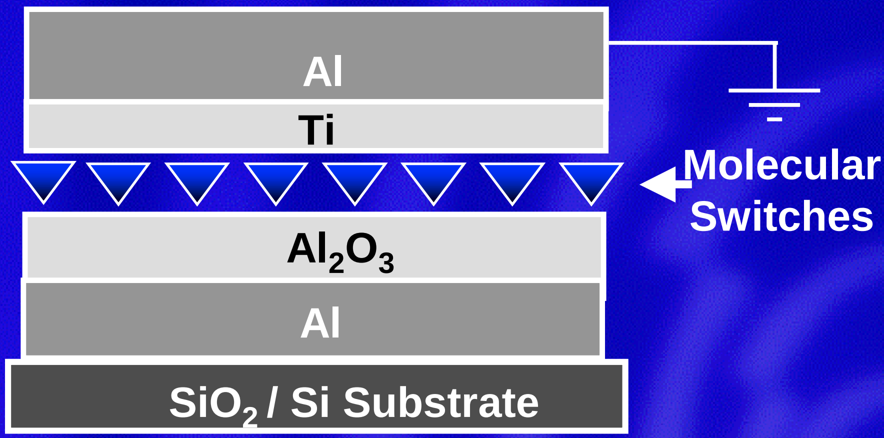


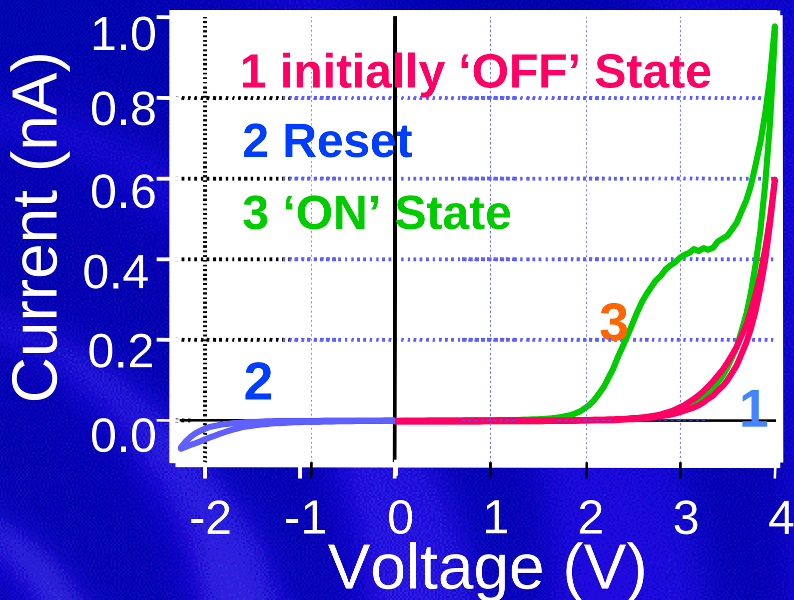
CONVENTIONAL MICROTRANSISTOR (a) has three terminals, known as the source, gate and drain. A positive voltage applied to the gate draws electrons to the insulator (b), enabling current to flow from the source to the drain. A molecule based on three benzene rings (c) was also used to switch an electric current. The center ring had asymmetric fragments, enabling it to be twisted by an electrical field (d). With a specific voltage applied, the electrical field twisted the molecule and permitted current to flow.

- Electric field modulates conductivity
- For an all polymer integrated circuit example see:
- Drury et al., Appl. Phys. Lett. 73< 108 (1998)

Memory device concept







Eicosanoic Acid ($C_{20}O_2H_{40}$)

Basic device elements:

- Monolayer molecular film: 0.5-3nm
- Cross bar electrodes

Edwards (HP): Presentation on Molecular electronics, 2001

Many remarkable properties uncovered but many issues remain

- Actively being investigated for transistors, memory devices, optoelectronics and displays
- Many molecules have been identified and are under study
  - Some have hysteresis suggesting potential uses as Non Volatile Memory devices
  - Many have fluorescent or phosphorescent properties
- Methods for self assembly of single molecular layers proposed
- May prove useful for low performance, low cost devices

Summary

- Converged devices will deliver computing and communications services anytime, anywhere
- More functional integration: On chip & multi-chip
- Chip interconnect and power challenges require innovative solutions
- Product architectures will diversify to serve new usage models including wireless-enabled ones
- Nanotechnology opens new process, materials, and device options to extend silicon scaling
- Process/packaging integration will be key to implementing new technology options
- Needs and opportunities for research and engineering will grow

Muchas Gracias

Thank You